An 8-bit 100KS/s Low Power Successive Approximation Register ADC for Biomedical Applications

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Abstract

This paper presents an 8-bit 100KS/s successive approximation register (SAR) analog-to-digital convertor (ADC) in SMIC 0.13 μm 1P8M process for biomedical applications. This ADC is implemented with sub-circuits consuming no static power, thereby preserving the desired low power characteristic. According to the measured results, the SAR ADC has a signal-to-noise distortion ratio (SNDR) of 49.2 dB, and the spurious free dynamic range (SFDR) of 63 dB for a 9.37 kHz full-scale input sinusoidal wave at a 100 kHz sampling rate. The effective number of bit (ENOB) is 7.8 bits. The differential nonlinearity (DNL) is in the range of -0.15/+0.15 LSB whereas the integral nonlinearity (INL) is within -0.35/+0.23 LSB. The total power is 3.2uW and the figure of merit (FOM) is 143 fJ/conversion-step.

1. Introduction

Thanks to the development of the integrated circuit technology, system of chips (SOC) has taken place of the discrete devices in different kinds of application fields for the sake of lower power dissipation, smaller area and lower cost. In the biomedical application areas, most of the bio-systems are portable or wireless implantable devices, which require the power dissipation to be as low as possible to extend the duration of the system [1][2]. In general, such a bio-system consists of a analog-to-digital convertor (ADC) transforming analog signals which represent the physical features of human body to digital signals for the subsequent signal processing.

Compared with other ADC architectures, SAR ADC is most appropriate for biomedical applications because of its extremely low power dissipation [3]. Though SAR ADC achieves moderate speed and medium resolution, it meets the specifications of bio-systems which deal with kinds of low-frequency bio-signals in noisy human body environment. In order to reduce the power dissipation of the SAR ADC, passively complementary NMOS and PMOS switches and a capacitor digital-to-analog array are adopted in this design. A dynamic comparator with no static power and much lower offset is implemented in the proposed SAR ADC.

The rest of the paper is organized as follows. Section II presents the specifications of the SAR ADC and details its circuit implementation. Section III presents measurement results. Section IV gives a brief conclusion of the paper.

2. Design of the SAR ADC

The bio-signals of human body such as electrocardiography (ECG), electroencephalography (EEG) and electromyography (ECG) along with output signals for biosensors and transducers are instinctively low-frequency, so there is no need to design high speed ADC in bio-systems [4]. Moreover, bio-signals occur in a relatively noisy human body environment, thus the resolution of the ADC for biomedical application systems is usually 8 to 10 bits. Thus, an 8-bit 100KS/s low-power SAR ADC is designed for the biomedical applications systems.

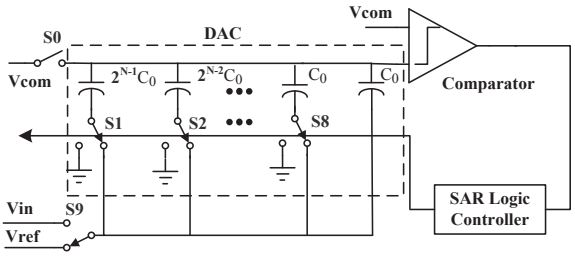

Figure 1. Architecture of proposed SAR ADC

In general, a fully-differential circuit structures achieves better common-mode noise rejection and less distortion, but its power dissipation is almost twice as large as that of a single-end structures. Because our SAR ADC focuses on a moderate resolution, all the circuit components are implemented as single-ended structures in order to reduce power. Figure 1 depicts the architecture of the proposed SAR ADC, which consists of sample-and-hold (S/H) switches, a binary-weighted DAC, a dynamic comparator and a successive approximation register logic controller for a low-power circuit implementation.

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2.1 S/H switches

There are two different types of switches (Figure 2): switch S0, which connects to the gate of the comparator and upper plates of the capacitor arrays; switch S1~S9, which directly or indirectly connect to bottom plates of the capacitor arrays. All these switches are implemented by passively complementary NMOS and PMOS switches to save the power dissipation and to achieve a nearly constant on-resistance to increase linearity. In addition, switch S0 would suffer from non-ideal effects such as channel charge injections and clock feedthrough, which might induce distortion of the sampling circuit. The distortion will decrease the actual resolution of SAR ADC. As shown in Figure 2, dummy MOSFETs, M3 and M4, whose dimensions are half of M1 and M2, are added in order to compensate for the nonlinearity error. It meets the accuracy requirements for 8-bit resolution.

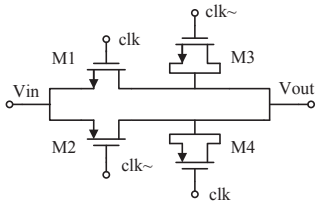

Figure 2. Complementary sampling switch S0 with dummy MOSFETs

2.2 Comparator

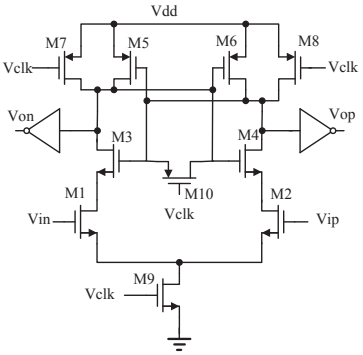

Figure 3. Dynamic comparator circuit

A proposed low-power and low-offset dynamic comparator is implemented in this work (Figure 3). Dynamic comparator consumes no static current and very little dynamic power, which is suitable for low-power design. The comparator has two operation phases: the reset phase and the comparison phase. When V_{clk} is low level, the comparator is in reset phase. The nodes V_{op} and V_{on} are reset to ground. The comparator consumes no static power because the tail NMOS M9 is off. M10 is inverted to avoid hysteresis of previous clock period. When V_{clk} is high level, the comparator is in comparison phase. The node voltages of M3 and M4's drain get lower and lower at unequal rate because of the differential stimulus input signals V_{ip} and V_{in}. Then the positive feedback M4-M6 evaluates the distinction of node voltages of M3 and M4's drain and latches the comparator. When the output of comparator is stable, no current flows from V_{dd} to ground.

The major issue of dynamic comparator is random offset including static offset and dynamic offset [5]. The mismatch of threshold voltage, the mismatch of ratio of width and length and the mismatch of process parameters would probably contribute the random offset. Obviously, offset could be decreased by using larger dimensions MOSFETs. However, large parasitic capacitance introduced by larger MOSFETs would consume much more power, which betrays our goal of low-power design. Our strategy is to find the main contributors to offset and to explore the tradeoffs in comparator design such as offset, area and speed. Among all the MOSFETs in the comparator, the input differential pair, M1 and M2, have the biggest influence on the input-inferred offset, as shown in the following equation:

$$V_{\text{off}1,2} = \Delta V_{\text{T}} + \frac{V_{\text{gs}} - V_{\text{T}}}{2}\left(\frac{\Delta R_{\text{L}}}{R_{\text{L}}} + \frac{\Delta\beta}{\beta}\right) \quad (1)$$

Where ΔV_T denotes the threshold voltage mismatch, V_{gs} represents the gate-source voltage of M1 and M2, $\Delta R_L/R_L$ and $\Delta\beta/\beta$ are load resistance mismatch and process mismatch, respectively. The input-inferred offset varies when the overdrive voltage (V_{gs}- V_T) of input pair changes. Thus, the dimensions of M1 and M2 should be largest among the whole comparator. However, the mismatch of M3-M6, could be attenuated by voltage gain of M1 and M2 to input-inferred offset, so their width and length should be optimized in medium dimensions. Finally, the controlling MOSFETs, M7, M8 and M10, could be optimized as small dimensions, which don't have much influence on the offset. In addition, the offset of comparator is influenced by load capacitance. Two inverters are inserted on the output nodes of comparator to isolate the effect of the probable unequal load capacitance. What's more, these two inverters could also shape the output waveform of the comparator.

We also carefully considered the speed limit of the comparator. For a 100 KS/s sampling rate o f the 8-bit ADC, the speed of the comparator must be larger than 1 MHz, because the SAR ADC needs ten clock periods to complete a conversion step. However, the settling time of the comparator should be seven times its time-constant within the 0.1% accuracy. Thus a comparator with propagation less than 100 ns is designed.

2.3 Digital-to-Analog convertor

The DAC in the SAR ADC can be implemented by different kinds of structures, such as resistor string, current-steering and capacitor array. Among these structures, the capacitor-array DAC consumes no static power. In addition, the fabrication process mismatch of

the capacitor is much smaller than resistor. A binary-weighted switched-capacitor array is designed in this work (Figure 1). Switch S0-S9 are controlled by the signals generated by the SAR logic controller and the binary-weighted capacitor is a combination of unit capacitor C_0. The value of the C_0 should be balanced between power, area, noise and mismatch.

The binary-weighted switched-capacitor array consumes little power and occupies small silicon area. On the other hand, it suffers from larger DNL and INL error by nature [6]. At the most significant bit decision, 2^{N-1} unit capacitors turn on/off and 2^{N-1}-1 other independent capacitors turn off/on. Assuming a Gaussian distribution for the unit capacitor with a standard deviation σ(C), this step has a σ(ΔC) determined by

$$\begin{aligned}\sigma^2(\Delta C) &= \sigma^2(2^{N-1}\cdot C-(2^{N-1}-1)\cdot C)\\ &= 2^{N-1}\sigma^2(C)+(2^{N-1}-1)\sigma^2(C)\\ &= (2^N-1)\sigma^2(C)\end{aligned} \quad (2)$$

$$\Rightarrow \sigma(\Delta C)=\sqrt{2^N-1}\sigma(C)=\sqrt{2^N-1}\frac{\sigma(C)}{C}LSB \quad (3)$$

σ(ΔC) is a good approximation for the DNL error. The $\sigma^2(\Delta C)$ at the most significant bit transition is approximately larger than any other bit transitions. And the parameter σ(C)/C in the preceding formula is described by

$$\frac{\sigma(C)}{C}=\frac{S}{WL} \quad (4)$$

Where W and L represent the width and length of the unit capacitor, respectively. S is a process dependent constant. In the SMIC 0.13μm 1P8M process, the value of S is 0.496*μm^2. In this paper, a metal-insulator-metal (MIM) unit capacitor of 40fF is implemented to trade off power consumption and mismatch, which induces the worst DNL of 0.2 LSB. In this situation, thermal noise kT/C of the capacitor array has barely effect on the resolution of the ADC.

2.4 Successive approximation register logic controller

The SAR logic controller generates signals to control S/H switches, comparator and DAC. Ten clock cycles are required to complete a conversion step. The first cycle is sampling cycle. Then the SAR logic controller decides to produce the digital outputs D8-D1 in the next eight clock cycles. The ADC exports the 8-bit digital output in the last cycle.

The SAR logic controller is realized by standard CMOS logic gates, whose power consumption is approximately

$$P_{SAR}(V_{in})=f_{clk}\cdot V_{dd}^2\cdot C_{tot}\cdot\alpha(V_{in}) \quad (5)$$

Where f_{clk} denotes the clock frequency, C_{tot} represents the total capacitance of the circuit nodes including parasitic capacitor and load capacitor of switches, and $\alpha(V_{in})$ is the switching activity factor which depends on the input signal V_{in} [7]. Obviously, the circuit consumes much less power when the V_{dd} is set lower. And the logic gates is implemented as small as possible in order to decrease the digital power.

3. Meaurement Ruselts

The SAR ADC is fabricated in a SMIC 0.13 μm 1P8M process. The SAR ADC is a part of an integrated mixed-signal biosensor chip, so the chip photograph of SAR ADC shows no PADs (Figure 4). The core size of SAR ADC is 0.08 mm^2.

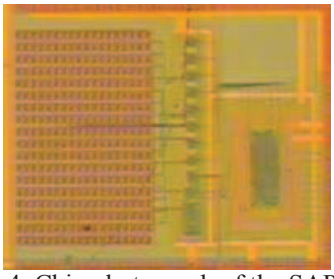

Figure 4. Chip photograph of the SAR ADC

3.1 Static measurement

Figure 5 illustrates the measured differential nonlinearity (DNL) and the integral nonlinearity (INL). The input signal with 377 Hz and 1.2V_{pp} sinusoidal wave is fed into the SAR ADC, and the sampling rate is 100 kHz. The measured results show that DNL is in the range of -0.15/+0.15 LSB whereas the INL is within -0.35/+0.23 LSB.

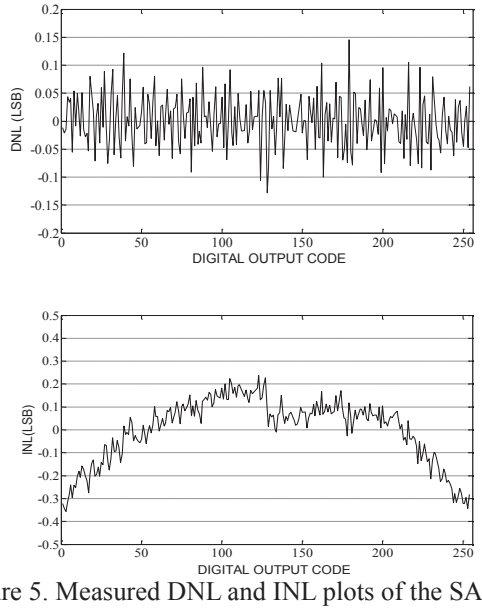

Figure 5. Measured DNL and INL plots of the SAR ADC

3.2 Dynamic measurement

A full scale 9.37 kHz sinusoidal wave spectrum measured at 100 kHz sampling rate is shown in Figure 6. The signal-to-noise distortion ratio (SNDR) is 49.2 dB and the spurious free dynamic rage (SFDR) is 63 dB. In addition, the effective number of bit (ENOB) is 7.8 bits.

Figure 7 illustrates the measurement results of the ADC's ENOB versus different frequencies of input sine-wave signals. The ENOB does hardly degrade even with the frequency close to the Nyquist frequency. In other word, the test results imply that this ADC achieves a wide effective resolution bandwidth (ERBW).

The figure of merit (FOM) dictates the energy required to accomplish an effective conversion step of an ADC. The FOM is defined as

$$FOM = \frac{Power}{2^{ENOB} \cdot f_{sample}} \quad (6)$$

The measured AD power dissipation is 3.2μW at a 1.2V supply voltage at 100 kHz sampling rate, thus the FOM of the SAR ADC is 143 fJ/conversion-step.

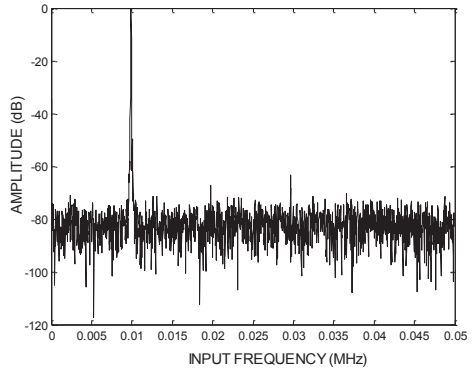

Figure 6. Measured output spectrum of SAR ADC with full-scale 9.37 kHz sinusoidal input waveform

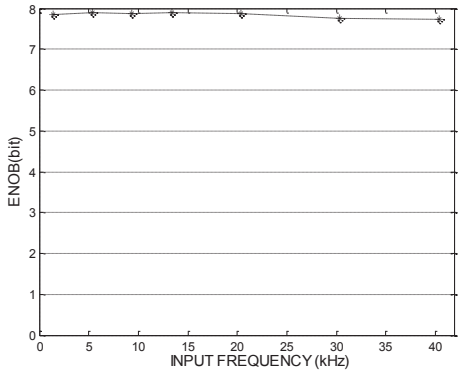

Figure 7. Measured ENOB versus different input sinusoidal frequencies

4. Conclusion

An 8-bit 100KS/s low power SAR ADC is implemented in SMIC 0.13 μm 1P8M process for biomedical applications. In order to decrease the power consumption, all switches are designed by passively complementary NMOS and PMOS which could easily meet the accuracy of an 8-bit resolution. A dynamic comparator is adopted for the sake of reducing power dissipation. The dimensions of comparator are carefully designed with tradeoffs between power, offset and speed. The value of unit capacitor C_0 of DAC is carefully calculated for power dissipation and mismatch considerations. The measurement results show that the ADC with 937 kHz full-scale input sinusoidal wave can achieve ENOB of 7.8 bits under 3.2μW which is very suitable for biomedical applications.

Acknowledgments

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References

[1]Kyong Ho L, Sun-Yuan K, et al. Improving kernel-energy trade-offs for machine learning in implantable and wearable biomedical applications, Acoustics, Speech and Signal Processing, IEEE International Conference on, p.1597-1600 (2011)

[2]Hyejung K, Sunyoung K, et al. A Configurable and Low-Power Mixed Signal SoC for Portable ECG Monitoring Applications, Biomedical Circuits and Systems, IEEE Transactions on, p.1-11 (2013)

[3]Michael S, Bernhard B, et al. An ultralow-energy ADC for Smart Dust, Solid-State Circuits, IEEE Journal of , p.1123- 1129 (2003)

[4]Shuenn-Yuh L, Chih-Jen C, et al. A 1-V 8-bit 0.95mW successive approximation ADC for biosignal acquisition systems, Circuits and Systems, IEEE International Symposium on, p.649 – 652 (2009)

[5]Jun H, Sanyi Z, et al. Analyses of Static and Dynamic Random Offset Voltages in Dynamic Comparators, Biomedical Circuits and Systems, IEEE Transactions on, p.911-918 (2009)

[6]Anne B, Marc B, Anne Van den Bosch, et al. A 10-bit 1-GSample/s Nyquist current-steering CMOS D/A converter, Solid-State Circuits, IEEE Journal of, p. 315-324 (2001)

[7]Hao-chiao H, Guo-Ming L, et al. A 65-fJ/ conversion-step 0.9-V 200-kS/s rail-to-rail 8-bit successive approximation ADC, Solid-State Circuits, IEEE Journal of, p. 2161- 2168 (2003)