A CMOS Passive Mixer-First Receiver Front-end for UHF RFID Reader

Zhiheng Lin, Xi Tan*, Hao Min

ASIC & System State Key Laboratory, AUTO-ID Laboratory of Fudan University
Room 365, Microelectronic Building, NO.825 Zhangheng Rd, Pudong District,
Shanghai, 201203, China
* Email: tanxi@fudan.edu.cn

Abstract—A CMOS passive mixer-first receiver front-end for UHF RFID Reader is presented in this paper. Instead of LNA input structure, we choose single-balanced passive mixer as the input stage to improve compression point, and can handle the large jammer noise from the leakage of the transmitter. The transimpedance amplifiers are followed by the mixers to provide enough gain and suppress the noise behind. We also use complex impedance match at baseband to control the real and imaginary part of the antenna equivalent impedance. This can leave out the matching network off chip. The receiver front-end circuit is designed in SMIC 0.13μm CMOS process.

Index Terms – RFID reader; mixer-first; baseband Amplifier; impedance matching

1. Introduction

Nowadays, due to part of general identification procedure, radio frequency identification (RFID) systems are becoming indispensable in logistics, manufacturing, storage management, etc. Ultra-high frequency (UHF) RFID applications specifically attract widely attention, as the communication distance and reading speed of which are moderate. Passive tags are now growing rapidly in daily life because of the small volume and low cost. However, the demand of performance of reader is so high that high performance discrete devices are still needed, which makes them not portable and the cost keep price up.

In a passive tag UHF RFID system [1], an electromagnetic wave is transmitted from the reader and then scattered back together with the tag's information. The operating frequency of UHF is from 860MHz to 960MHz, and the typical working distance is less than 10 meters. As for reader, scaling down the area, cut down the power and improve the performance such as linearity and low noise are the main challenge. R1000 [2] from Intel gave a good attempt using SiGe, supplying with 5V voltage, which evidenced single-chip reader became to practical stage. Another single-chip solution [3] from research institutes implemented in CMOS process, but with two separate antennas.

This paper describes a CMOS passive mixer-first receiver front-end for UHF RFID Reader with complex impedance match at baseband, which scales down the matching network off chip. The whole architecture shows in section 2. Section 3 presents the blocks in detail, including passive mixer, baseband amplifier, and impedance matching network. Then, the simulation results and layout will be displayed in section 4. Section 5 is the summary.

2. Receiver Architecture

UHF RFID system is simply shown in Fig.1. In general, the system suffers from large leakage of the carrier because of insufficient Tx-Rx isolation, which is a continuous wave signal from a reader to supply passive tags' internal circuits. A circulator or a directional coupler is generally employed to isolate the transmission path from reception path, or else a dual-antenna system is introduced. But both of the attempts are difficult to achieve the isolation more than 25dB. So the leakage from power amplifier of the transmitter to receiver is inevitably large thanks to the Tx-Rx coupling.

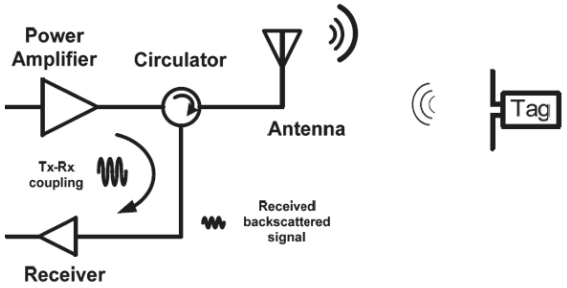
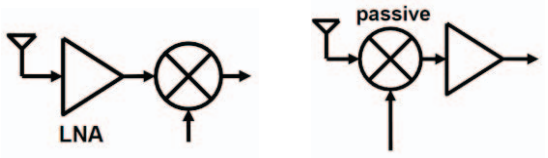


Figure 1. Sketch of UHF RFID system

To get high spurious free dynamic range (SFDR), which characterizes the maximum distance between signal and noise distortion, the desires of the receiver are low noise and high linearity [4]. If we choose traditional LNA-first structure shown in Fig 2(a), low noise can be achieved easily, but large jammer noise will be amplified by LNA so that the front-end is soon saturated. Then we try passive mixer-first structure as Fig 2(b) shows, providing high linearity. Though it is at the cost of

978-1-4673-6417-1/13/$31.00 ©2013 IEEE

conversion loss, the amplification can be postponed to IF. It is a good method to handle large jammer noise, for passive mixer nearly provide no gain and jammer can be dealt with after down conversion. Then conversion gain can be offered by baseband amplifier.



(a) (b)

Figure 2. (a) LNA-first structure (b) Mixer-first structure

The implemented receiver front-end is shown in Fig 3. The proposed direct-conversion architecture includes a single-balanced passive mixers driven by an on-chip clock divider generating the quadrature clock phases. Gain is offered by baseband amplifiers behind. It also provide tunable baseband impedance matching which is introduced in detail in section 3.3, without matching network at RF port.

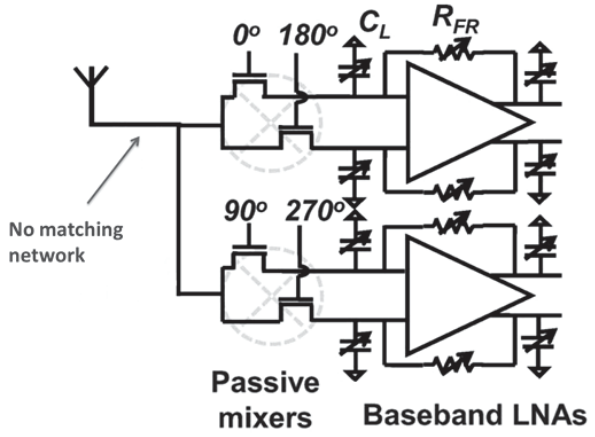


Figure 3. Receiver front-end architecture

3. Circuits Implementation

The receiver chip was designed in SMIC 0.13μm 1P8M CMOS process. It consists of passive mixers and baseband amplifiers.

3.1 Passive Mixer

Due to the large leakage, the input stage should have a high input compression point and limited gain. So a passive mixer was chosen. The attempt that connecting the antenna directly to a passive mixer without RF LNA can provide considerable benefit, such as high linearity, low flicker noise, and low power consumption. We prefer single-balanced passive mixer to double-balanced mixer, so we can leave out the trouble from balun and provide differential conversion gain.

Passive mixers are driven by 50% duty cycle four-phase Lo frequency, in voltage switching mode as shown in Fig 4.

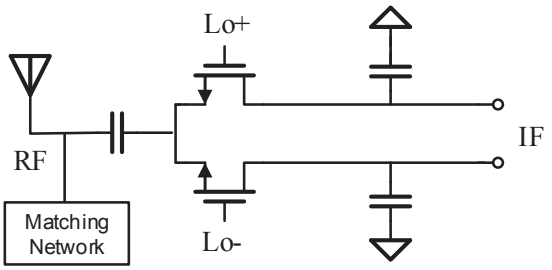


Figure 4. Receiver front-end architecture

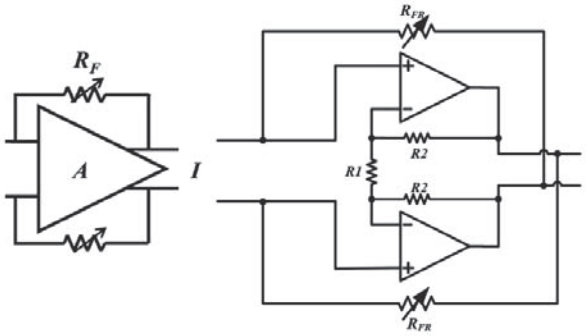
3.2 Baseband Amplifier

Following the passive mixer, there is a feedback amplifier at IF, the equivalent input impedance is R_B as shown in Fig 5(a).

$$R_B = \frac{R_F}{1+A} \tag{1}$$

However, if the amplifier is open-loop structure, the open-loop gain is not stable because of supply voltage swing, the corner and temperature, etc. So a closed-loop amplifier which is double in and double out is introduced. The gain of the operational amplifier is only determined by the ratio of the resistances which is stable. The expression of gain A is as below.

$$A = 1 + \frac{R_2}{R_1 / 2} \tag{2}$$



(a) (b)

Figure 5. (a)Feedback amplifier (b)Improved structure

A transistor-level schematic of the proposed baseband amplifiers is shown in Fig. 6. The amplifier is a simple CMOS OTA. It consists of a fully differential input PMOS pair with NMOS loads. We chose PMOS transistors as the input pair, 3V as the supply voltage to handle the large input and output voltage swing, and we have to enlarge amplifier transistors with long channels to reduce the flicker noise. The OTA can provide enough Open-loop gain and GBW.

We implemented the feedback matching resistor R_B by wrapping feedback loops around both paths. The

feedback actually are resistor arrays, which consist of 8 resistors each controlled by switches, connected to the input gates, in series with a source follower to buffer the output.

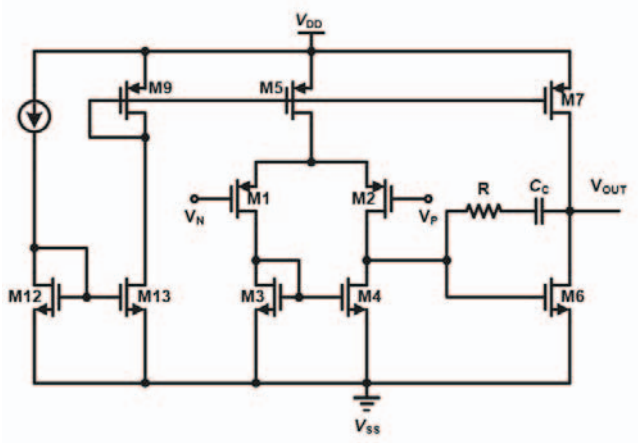


Figure 6. Transistor-level schematic of baseband amplifier

3.3 Complex Feedback and Impedance Matching

At RF port, designing to match a constant, purely real antenna impedance of 50Ω is our target. However, the equivalent input impedance of antenna can vary in different environment or at different operating frequencies. Moreover, the presence of parasitics on pads, the PCB, package, and bond wires inherently make the effective antenna impedance complex. Furthermore, it is a reduction of cost to be free from matching network off chip. Those above are the main goals we try complex feedback and baseband impedance matching.

Here we connect feedback resistances from the output of I-channel of the baseband amplifier to the input of Q-channel, and vice versa [5]. The feedback paths can present a 90° phase shift of the original signals back to the amplifier inputs, which translates to complex impedance presented to the antenna port through the passive mixer. And we can realize positive imaginary and negative imaginary through different way of connection.

Through analysis of the circuit in Fig 7, we get an expression for the new baseband impedance Z_B where the real part still mostly depends on the real feedback resistor R_{FR}, and the imaginary component is decided by the value of the resistor R_{FI}. It is noted that equivalent resistance R_B from (1) will change to Z_B.

$$Z_B = [(\frac{1+A}{R_{FR}} + \frac{1}{R_{FI}}) \pm j\frac{A}{R_{FI}}]^{-1} \qquad (3)$$

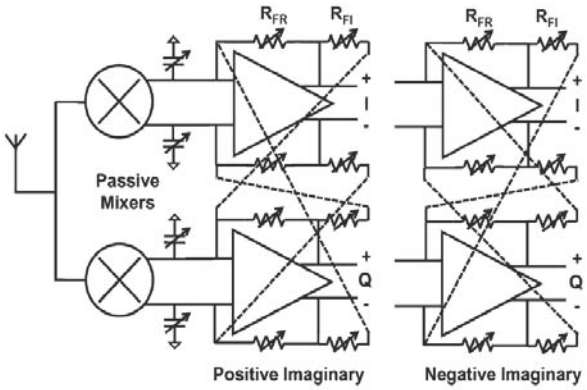


Figure 7. Receiver front-end schematic with baseband complex feedback

In order to see the effects of complex feedback, we simulate the receiver to receive an RF frequency around 900 MHz and swept the RF frequency.

First we use ideal operational amplifier. We tuned the impedance match with the real feedback resistor to offer a desired deep S11 notch, without setting up the complex feedback.

We then turn on the complex feedback path with a positive R_{FI} value and swept the RF frequency again, as expected this shifted the IF frequency of the optimum S11. The results are shown in Fig 8.

R_{FR} and R_{FI} are both resistance arrays controlled by switches. We can easily handle the baseband impedance matching through tuning the switching.

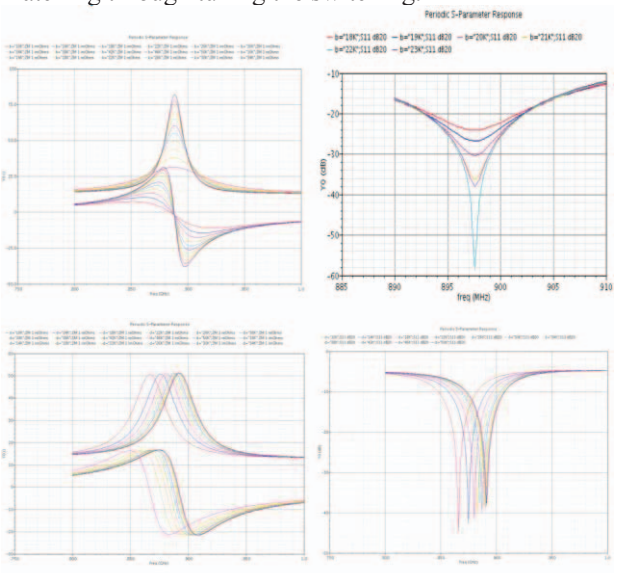


Figure 8. Simulated Z_B and S11 for varying R_{FR} and R_{RI}

And when using the operational amplifier we just mentioned, we can also get a good impedance matching through tuning the resistance.

4. Simulation Results of the Receiver

4.1 Simulation results

The proposed receiver has been simulated with Cadence's Spectre simulator. The results are shown in Table 1.

We got the 5dB compression point is greater than -10dBm. When input carrier signal increases, output power no longer increases. We add an attenuator weakening jammer by -15dBm.

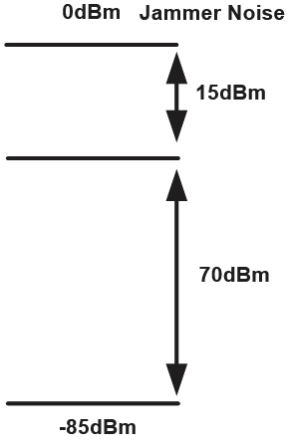


Figure 9. Spec of signal system

The gap between jammer noise leaked from transmitter and desired signal generally reaches to 65 dBm. We assume it 70dBm as shown in Fig 9. Jammer noise is around 0dBm. SNR is about +15dB. Let integral noise bandwidth 100kHz, and we get the noise figure is no larger than 24 referring the equation below.

$$P_{in,\min} = -174dBm/Hz + NF + 10\lg B + SNR_{\min} \quad (4)$$

Table 1. Simulation results of the Receiver Front-end

Parameter	Simulated Value
Process	SMIC 0.13μm CMOS 1P8M
Conversion Gain	21.8dBm
Noise Figure	21.88dB (integrated from 100Hz~100KHz)
1dB Compression point	- 8.37dBm
IIP3	2.96dBm
I_{total}	7mA

Noise figure and other parameter can meet the spec we defined. Meanwhile, baseband impedance matching can be achieved through tuning the feedback resistance arrays.

4.2 Layout Design

The chip is designed in SMIC 0.13μm CMOS 1P8M. The layout design can be seen in Fig 10. In order to generate four-phase quadrature clock signal, we also design a frequency dividers, shown in the left of the layout. Passive mixers and baseband amplifiers are displayed in the right. The total area is 1.45mm^2 including dividers and pads.

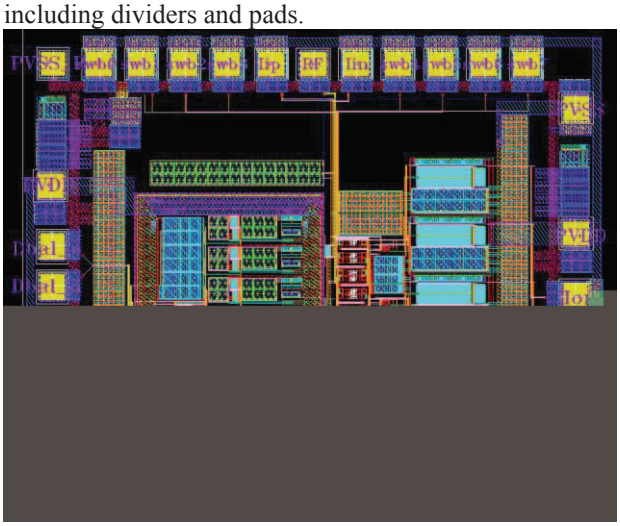


Figure 10. Layout of the design

5. Summary

The passive mixer-first receiver front-end with complex impedance match at baseband has been presented. The conversion gain of passive mixer and baseband OTA can reach more than 20dB. The 1dB compression point is -8.37dBm, and IIP3 is 2.96dBm. Noise figure is around 22dBm. So it is suitable to be used in UHF RFID reader. The complex impedance match was introduced. By tuning the resistance array, we can get a good impedance match at the RF port free from the trouble of match network off chip. The chip has been taped out and waiting for testing.

Acknowledgments

This work is supported by National High Technology Research and Development Program (No.2011AA010404), and General Program for International Science and technology cooperation projects of China (NO.2010DFB13040).

References

[1] K. Finkenzeller. "RFID Handbook". New York: Wiley (1999)

[2] Scott, C., Issy, K., Marc, L., Jan, R., David, W., Jonas, J., and Peter, J. "A 900MHz UHF RFID reader transceiver IC", IEEE JSSC, vol. 42, No. 12, (2007)

[3] W. Wang, S. Lou, K. Chui, et al, "A Single-Chip UHF RFID Reader in 0.18um CMOS, Custom", Integrated Circuits Conference, pp.111-114, (2007)

[4] M. Soer, E. Klumperink, Z. Ru, F. E. van Vliet, and B. Nauta, "A 0.2-to-2.0 GHz 65 nm CMOS receiver without LNA achieving 11 dBm IIP3 and 6.5 dB NF," IEEE ISSCC, vol. 52, pp. 222–223. Feb. (2009)

[5] Caroline Andrews, and Alyosha C. Molnar, "A Passive Mixer-First Receiver with Digitally Controlled and Widely Tunable RF Interface", IEEE JSSC, vol. 45, No. 12, (2010)